REMARKS

This application has been carefully reviewed in light of the Office Action dated February 22, 2006. Claims 1 to 3, 5 to 8 and 10 remain in the application. Claims 4 and 9 have been canceled. Claims 1, 2, 6 and 7 are the independent claims. Reconsideration and further examination are respectfully requested.

Applicant thanks the Examiner for the indication that Claims 2 to 4 and 7 to 9 contain allowable subject matter. In keeping with this indication, Claims 2 and 7 have been rewritten in independent form. Additional changes have been made to Claims 2 and 7 in a manner not believed to affect their allowability. Accordingly, independent Claims 2 and 7 are believed to be in condition for allowance.

Claims 1, 5, 6 and 10 were rejected under 35 U.S.C. § 103(a) over U.S. Patent 6,510,474 (Stracovsky) or over U.S. Patent No. 6,212,611 (Nizar) in view of an allegedly well-known feature. In response, independent Claims 1 and 6 have been amended to include the language of allowable Claims 4 and 9, respectively. In making these amendments, however, the subject matter of intervening Claims 2 and 3 (and of Claims 7 and 8) has been omitted. Despite these omissions, it is believed that amended Claims 1 and 6 define over the applied art, as explained in more detail below.

Claim 1

The invention of Claim 1 generally concerns an arbitrator for reordering access requests to a memory system. A transaction buffer buffers access requests, and a mapping table maps input and output counter values to locations in the buffer. Among its many features, the invention of Claim 1 includes the features of (i) counting access requests received by an arbitrator using an input counter, (ii) mapping the input counter such that the input counter points to a transaction buffer location where a next received

access request is to be placed, and (iii) filling locations in the transaction buffer in the order that access requests issued from the locations in the transaction buffer.

Referring specifically to claim language, independent Claim 1 as amended is directed to an arbitrator for reordering access requests to a memory system to reduce memory system conflicts. The arbitrator includes a transaction buffer for buffering the access requests, an input counter for counting access requests received by the arbitrator, an output counter for counting access requests issued by the arbitrator, and a mapping table for mapping the input counter and the output counter to respective locations in the transaction buffer. The arbitrator also includes a reordering unit for dynamically re-ordering entries in the mapping table such that the mapping of the output counter points to the access requests in an issue order wherein memory system conflicts are reduced. The mapping of the input counter maps to the location in the transaction buffer that is to be filled by a next received access request, and the locations in the transaction buffer are filled in the order that access requests issued from the locations.

In contrast, the applied art is not seen to disclose or suggest the features of Claim 1, and in particular is not seen to disclose or suggest at least the features of (i) counting access requests received by an arbitrator using an input counter, (ii) mapping the input counter such that the input counter points to a transaction buffer location where a next received access request is to be placed, and (iii) filling locations in the transaction buffer in the order that access requests issued from the locations in the transaction buffer.

As understood by Applicant, Stracovsky discloses re-ordering command and data packets in order to restore an original order of out-of-order memory requests. A best position in a command queue is calculated for each new incoming command by a reordering block coupled to the command queue. Read data is stored in a data queue while

the associated incoming commands are stored in their respective original order in a FIFO register included in a re-reordering block. The data is stored in its original order in a data queue while incoming data from the memory is stored in a read-data buffer included in the re-reordering block according to the order stored in the data queue. The stored commands are sent to the processor according to the order stored in the FIFO. See Stracovsky, Abstract.

Page 3 of the Office Action asserts that Stracovsky (Column 25, line 26 through Column 26, line 1) discloses buffering commands in a queue with a time factor, detecting collisions between the current command and the issued command, and reordering the commands.

However, Stracovsky is not seen to disclose or suggest at least the features of (i) counting access requests received by an arbitrator using an input counter, (ii) mapping the input counter such that the input counter points to a transaction buffer location where a next received access request is to be placed, and (iii) filling locations in the transaction buffer in the order that access requests issued from the locations in the transaction buffer.

In particular, while Stracovsky is seen to disclose counters, Stracovsky is not seen to disclose or suggest the claimed input counter. Specifically, Stracovsky's livelock counter register contains information about how many consecutive requests with higher priority can bypass requests with a lower priority. See Stracovsky, Column 8, lines 48 to 53. Stracovsky's "bank counter" records a number corresponding to whether a memory bank is open or closed. See Stracovsky, Column 11, lines 15 to 36. Finally, Stracovsky's replacement counter is updated based upon a pseudo-random counting scheme or "other appropriate schemes". See Stracovsky, Column 16, lines 51 to 55.

In contrast, Claim 1 features an input counter which counts access requests received by an arbitrator.

As Stracovsky is not seen to even disclose the claimed input counter, Stracovsky is also not seen to disclose or suggest the feature of mapping the input counter such that the input counter points to location in a transaction buffer where a next received access request is to be placed.

Stracovsky is also not seen to disclose or suggest the feature of filling locations in a transaction buffer in the order that access requests issued from locations in the transaction buffer. Rather, Stracovsky discloses inserting commands into a command queue at the first free position with the highest priority. See Stracovsky, Column 20, lines 45 to 48.

Nizar, for its part, is not seen to remedy the above-noted deficiencies of Stracovsky, since it is also not seen to disclose an input counter as claimed herein.

Accordingly, the applied art is not seen to disclose or suggest at least the features of (i) counting access requests received by an arbitrator using an input counter, (ii) mapping the input counter such that the input counter points to a transaction buffer location where a next received access request is to be placed, and (iii) filling locations in the transaction buffer in the order that access requests issued from the locations in the transaction buffer.

Therefore, independent Claim 1 is believed to be in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Claim 6

The invention of Claim 6 likewise generally concerns reordering access requests to a memory system. A transaction buffer buffers access requests, and a mapping

table maps input and output counters to locations in the buffer. Among its many features, the invention of Claim 6 includes (i) counting access requests received by an arbitrator using an input counter, and (ii) placing a next received access request in a transaction buffer at a buffer location pointed to by a mapping of the input counter.

Referring specifically to claim language, independent Claim 6 as amended is directed to an arbitration method of reordering access requests to a memory system to reduce memory system conflicts. The method includes buffering the access requests in a transaction buffer and maintaining a mapping table, the mapping table mapping an input counter and an output counter to locations in the transaction buffer. The method also includes dynamically re-ordering entries in the mapping table such that the mapping of the output counter points to the access requests in an issue order wherein memory system conflicts are reduced. Additionally, the method includes counting access requests received by the arbitrator using the input counter, and placing a next received access request in the transaction buffer at a buffer location pointed to by the mapping of the input counter.

As discussed above, the applied art is not seen to disclose or suggest at least the features of counting access requests received by an arbitrator using an input counter, and mapping an input counter such that the input counter points to a transaction buffer location where a next received access request is to be placed.

Accordingly, the applied art is also not seen to disclose or suggest the above-noted features of Claim 6.

Therefore, Claim 6 is also believed to be in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

No other matters being raised, the entire application is believed to be in condition for allowance, and such action is courteously solicited.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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